**DESIGN AND IMPLEMENTATION OF DSP-BASED THREE-LEVEL SIMPLIFIED SPWM MODULATION METHOD**

**Abstract**: The traditional three-level sinusoidal pulse width modulation (SPWM) requires two carriers to be compared with the modulating waveform to get the duty cycle, which can not be realized in a single-core DSP chip with high requirements. This paper proposes a three-level single-carrier SPWM waveform implementation method that does not increase the hardware cost. The scheme is based on the DSP28335 chip, using the DSP chip’s increment/decrement counting method, the comparison counter, and the DSP interrupts to compare the carrier waveform with the modulating waveform and get the PWM drive signals with different duty cycles. Simulation results show that compared with the traditional three-level SPWM algorithm, the proposed three-level simplified SPWM modulation not only controls the hardware cost, but also optimizes the bias of the intermediate capacitor voltage on the DC bus side, which reduces the harmonic distortion of the grid, shortens the time for the DC output voltage to reach the steady state, and verifies the effectiveness of the proposed modulation method.

**1. Introduction**

With the rapid development of current power electronic conversion technology and control theory, the voltage level and required power of electronic devices are increasing, and the traditional two-level converter can no longer meet the demand. The three-level converter, as an effective way to increase the power level, is widely concerned because of the increasing demand. Compared with two-level converters, three-level converters have certain advantages in terms of power quality, voltage withstand capability, output voltage harmonics, switching losses, and usage efficiency, so more and more scholars are devoted to the research of three-level converters [1-2]. In addition, one of the key technologies of high-power three-level converters is the PWM modulation strategy. The main common three-level converters are Vienna topology, NPC, ANPC, and NPC2 type topologies. Since the Vienna topology is widely used in high-power front rectifier circuits such as wind power generation and electric vehicle charging for the advantages of easy boost, few switching devices, and high conversion efficiency, the Vienna cannot meet the bi-directional flow of energy due to the topology [3-4]. On the contrary, NPC, ANPC, and T-type three-level topology can meet the bi-directional flow of energy, but compared to the T-type three-level topology, when there is current flow through the topology clamp midpoint, NPC-type three-level rectifier bridges imbalance of midpoint voltage [5]. ANPC structure for the control of the switch tube has strict timing requirements, and timing errors will bring a certain degree of danger [6].

The most common modulation methods for the PWM modulation strategy of high-power three-level converters are SPWM modulation and SVPWM modulation. The modulation principle of three-level SPWM is to use two same- phase triangular waveforms as carrier signals, comparing with the modulating signal to generate a PWM waveform [7-8]; the modulation principle of three- level SVPWM needs to go through coordinate transformation, judgment of sectors, calculation of sector action time and other steps

[9], which is more complex, especially when extended to multi-level, the complexity of the control algorithm rises at a cubic rate. However, since the three-level SPWM modulation has the disadvantage of low voltage utilization, compared with the three-level SVPWM modulation, the SPWM modulation can be equated to SVPWM modulation by the zero-sequence component approach or the FPGA-based third harmonic injection method can be used to improve the voltage utilization [10-11]. Compared with the irregular symmetric sampling method and the equivalent area method, symmetric sampling is simpler and faster, but the resources and costs are too high when multiple PWM waves need to be issued [12-13].

In this paper, a simplified SPWM modulation algorithm for a T-type three-level converter is proposed, choosing the T-type three- level topology with simple topology, convenient control, low cost, and conduction loss [14]. For the problems of traditional dual-carrier three-level SPWM and SVPWM, based on the analysis of dual-carrier three-level SPWM modulation and SVPWM, we take the strengths to complement the weaknesses, and three-level SPWM modulation is proposed. In this paper, we propose a simplified SPWM modulation with three levels based on the advantages and disadvantages of dual-carrier three-level SPWM modulation and SVPWM.

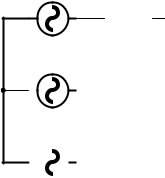
**2. T-type three-level main circuit topology and basic operating principle**

T-type three-level topology is one of the three-level NPC topologies. Compared with the other three-level NPC topologies, this topology eliminates the diode used to clamp, and there are no timing requirements in control. T- type three-level topology takes into account the traditional two -level three-phase six- switch converter energy bi-directional flow characteristics and three-level Vienna circuit high-efficiency characteristics, because this topology is a single phase shaped like the letter. Since this topology is shaped like the letter “T”, it is called T-type three level.

The T-type three-level rectifier circuit used in the paper is shown. In Figure 1, Ux (x=a, b, c) is the three-phase AC grid voltage; Lx (x=1, 2, 3, 4, 5, 6) is the AC side inductor; Rs is the parasitic resistance; Cx (x=1, 2, 3) is the AC side capacitor; QX1~4 (X=A, B, C) are the switching tubes; the DC side output capacitor is composed of filtering electrolytic capacitors C4 and C5 with equal capacitance; u1 and u2 are in the upper and lower position; u0 is the DC bus voltage.

L1 L4

Ua  Rs a ia



L2 L5

Ub  Rs b ib

L3 L6



Uc Rs ic c

C1 C2 C3

Rs Rs Rs



|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | QA1 | QB1 | QC1 |  | u1 | |  |  |
| Rs |  |  | QA3 | QA4 |  |  |
| A |  | C4 | |  |  |
|  |  |  |  |  |
| Rs |  | B | QB3 | QB4 | O | R | u0 |  |
|  |  |  |  |
|  |  |  |  |  |  |  |  |
| Rs |  |  | QC3 | QC4 |  |  |  |  |
| QA2 | QB2 | C |  | C5 | |  |  |
|  | QC2 |  |  |  |
|  |  |  |  |  |  | u2 |  |  |

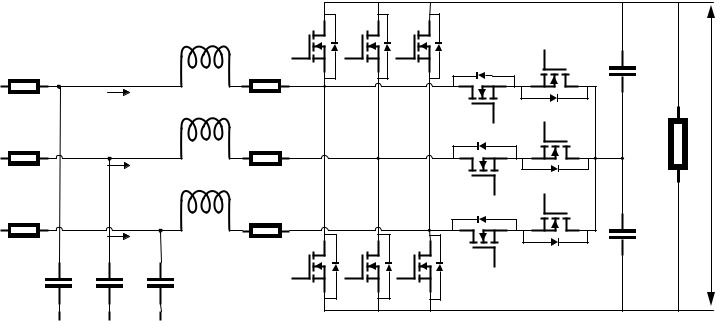


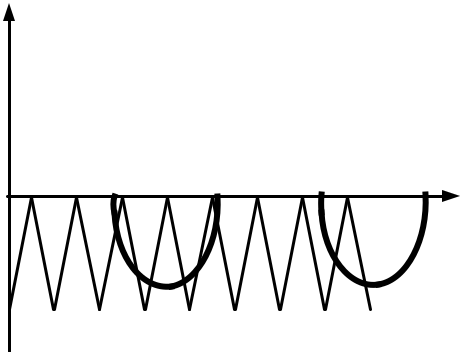
Figure 1. T-type three-level converter topology diagram

In Figure 1, for any one phase Ux (x=a, b, c), there are three modes of operation: Mode 1: QA1 and QA4 are on, QA2 and QA3 are off, and the voltage at the output is +0.5 Udc for Point O; Mode 2: QA3 and QA4 are on, QA1 and QA2 is off, and the voltage at the output is 0 for Point O; Mode 3: QA2 and QA3 are on, QA1 and QA4 is off, and the voltage at the output is -0.5 Udc for Point O. This analysis method can be extended to other three-phase cases.

**3. Conventional two-carrier three-level SPWM principle and limitations**

*3.1. Principle of conventional dual-carrier three-level SPWM*

The main method of conventional three-level SPWM modulation is to compare the sinusoidal modulating waveform with two triangular carriers in different periods. If the modulating waveform is larger than the carrier waveform, it is specified to output a high level, which corresponds to the closed state of the switching tube; on the contrary, it outputs a low level, which corresponds to the open state of the switching tube. This signal is used to drive the switching tube in the circuit. The dual-carrier modulation method is shown in Figure 2.



Amplitude

1

 ...

Time(s)

-1

Figure 2. Dual carrier modulation schematic

*3.2 Limitations of conventional three-level modulation*

The commonly used three-level modulation algorithms are mainly three-level SVPWM modulation and three-level two-carrier SPWM modulation, and the limitations of these two modulations are analyzed.

Firstly, the limitation of traditional dual- carrier three-level SPWM is that dual-carrier three- level SPWM needs to be equipped with dual-core above DSP chips, which has a high implementation cost. Secondly, the three-level SVPWM modulation algorithm includes large and small vector synthesis, sector judgment, sector working time calculation, and other operations, and its limitation is mainly reflected in the unreasonable large and small vector synthesis method. The limitation is that the unreasonable large and small vector synthesis method can cause bias in the midpoint voltage of the DC side capacitor, and the bias can cause damage to the DC side components. Therefore, how to improve the algorithm and the performance index in all aspects is a problem that we need to solve.

**4. Simplified three-level SPWM design and implementation**

*4.1 Simplified three-level SPWM design*

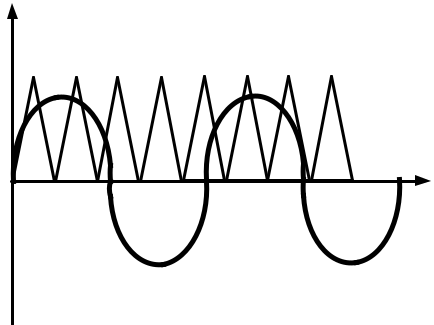
To cope with the above problems, this paper proposes a simplified three-level SPWM modulation technique. The core principle of simplified three-level SPWM is the same as that of dual-carrier modulation, but the number of carriers is reduced by the method of equivalent carriers, which reduces the hardware requirement for the master chip.

There are mainly two steps to equate the three-level dual-carrier SPWM with the simplified three-level SPWM. In this paper, we perform two steps to simplify the dual-carrier to obtain the simplified three-level SPWM modulation that can be equated to replace the three-level dual-carrier SPWM modulation.

As can be seen from Figure 3, the first step is simplified by first splitting the upper and lower carriers separately. When the modulating wave is greater than 0, the carrier and modulating wave are higher and lower than each other, so the duty cycle of the corresponding switch will be obtained according to the actual comparison. When the modulating wave is less than 0, the carrier wave is completely higher than the modulating wave at this time, so the corresponding switch state is completely disconnected until the next cycle starts the comparison again. The method is similar to the first cycle.

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Amplitude

1

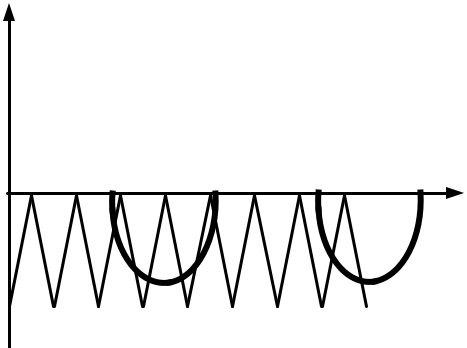
...

Time(s)

-1

Figure 3. Simplification in the first step (a)

From Figure 4, we can see that when the modulating wave is greater than 0, the modulating wave is completely greater than the carrier wave, so the corresponding switch state is completely closed. When the modulating wave is less than 0, the carrier wave and modulating wave are high and low, so the duty cycle of the corresponding switch will be obtained according to the actual comparison until the next cycle starts again, and the subsequent cycle comparison method is similar to the first cycle.



Amplitude

1

...

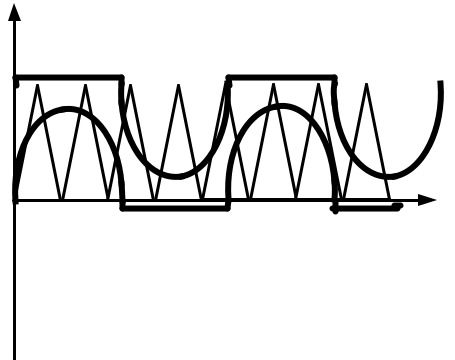
Time(s)

-1

Figure 4. Simplification in the first step (b)

The second simplification step is key. When the modulating waveform is larger than the carrier waveform in a certain period, the modulating waveform amplitude in that period is equivalent to twice the carrier waveform amplitude. When the modulating waveform is smaller than the carrier waveform in a certain period, the modulating waveform amplitude in that period is equivalent to minus twice the carrier waveform amplitude. This ensures that the corresponding PWM drive waveform in a certain cycle can guarantee the absolute closure or absolute disconnection of the switch, and there will be no interruption of the instantaneous closure of the switch, which largely reduces the switching loss.

The second step is simplified as shown in Figure 5.



Amplitude

1

Time(s)

-1

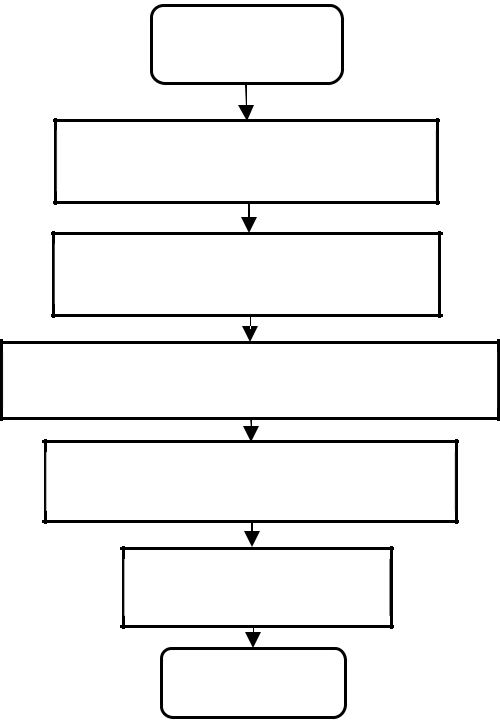
Figure 5. Simplification in the second step

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*4.2 Implementation of simplified three-level SPWM*

When implementing simplified three- level SPWM modulation based on the digital chip DSP28335, firstly, the chip peripherals, clock, and interrupt vector table should be initialized. Secondly, the EPWM module should be configured, and finally, the interrupt can be accessed for modulated waveform and carrier comparison. The flow chart of the main program of simplified three-level SPWM modulation is shown in Figure 6.



Start

Peripheral initialization

Epwm clock initialization

Interrupt vector table initialization

Epwm module initialization

Entry interrupt

End

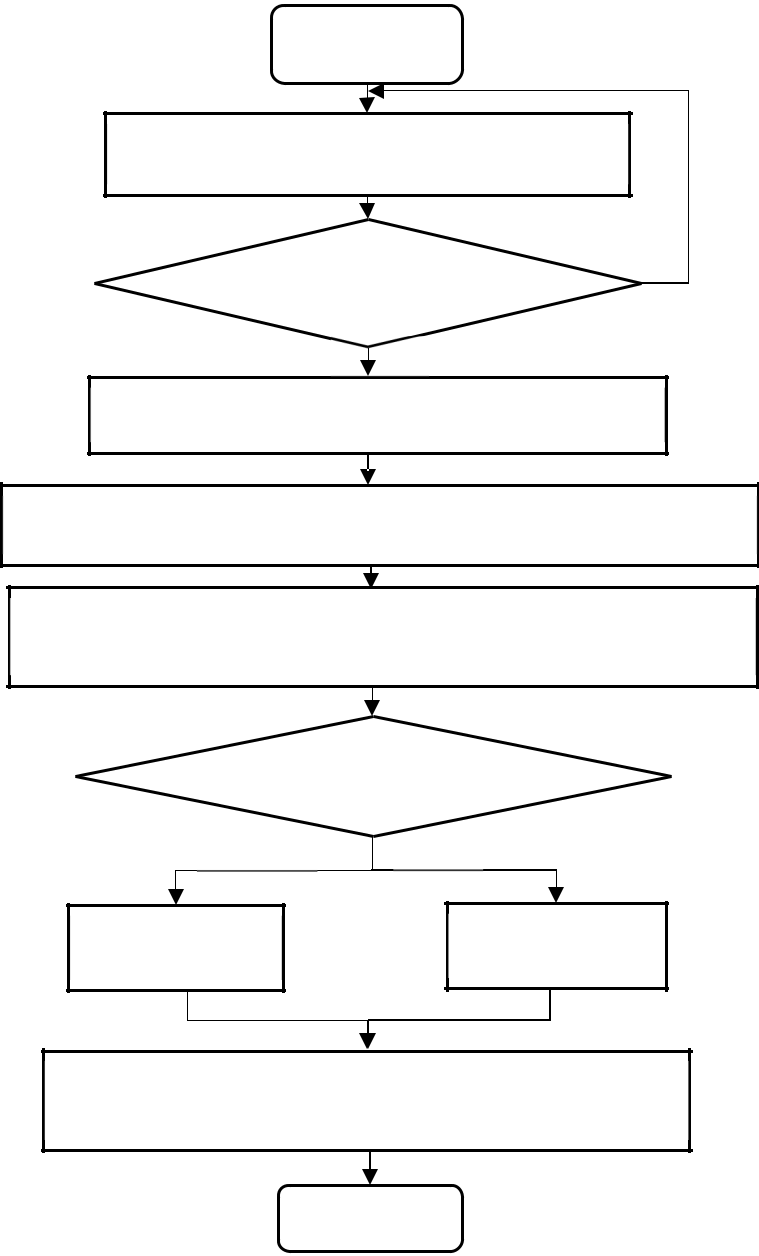
Figure 6. Main program flow chart of simplified three-level single-carrier SPWM modulation

For the actual modulated waveform and carrier comparison stage, the interrupts are written to the DSP, according to the DSP interrupt overflow law. When the output value is greater than the counter, the maximum will be output with the counter maximum; when the output value is less than zero, the output is zero. Before the comparison, the continuous sinusoidal modulated signal is firstly discrete and the counter is used to iterate through each discrete sinusoidal modulated signal. Secondly, the counting mode of the DSP counter TBCLK is set to increment and decrement counting mode. When the counter TBCLK starts to increment, counting from 0, and each time we add 1. When the counter reaches TBPRD, decrement counting starts, and each time we subtract 1. When the counter reaches 0 and TBPRD, the counter will be decremented by 1 each time, and the counter will start incrementing again when it reaches 0. The modulated waveform is replaced by the comparison submodule CMPx. Since the comparison submodule is mostly a fixed value, the product of the comparison submodule and the discretized sine waveform can replace the modulated waveform needed for comparison.

If the value of the TBCLK counting sub-module is greater than the CMPx of the comparison sub-module, it will be judged as incremental counting and output high level; if the value of the TBCLK counting sub-module is less than the CMPx of the comparison sub-module, it will be judged as decremental counting and output low level. The modulation interrupt flow chart of the simplified three-level single-carrier SPWM is shown in Figure 7.

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Start

Take the value of the counter (*i*=0、*i*++）

*i*>*N*(*N*=256)?

N

Calculate the value of *Uc*= sin(2\*π\**i*/*N*)

Y

Store the corresponding value in the comparison sub module

Adjust the counting mode to increase or decrease the

counting mode

TBCTR>CMPx?

Y N

High level

Low level

Get complementary PWM driving waveform by

inversion

End

Figure 7. Modulation interrupt flow chart of simplified three-level single carrier SPWM

**5. Simulation data and comparison**

To verify the feasibility of the above simplified three-level single-carrier SPWM method, a simulation model of the T-type three -level converter was built in the Matlab/Simulink simulation platform. The simulation parameters are shown in Table 1.

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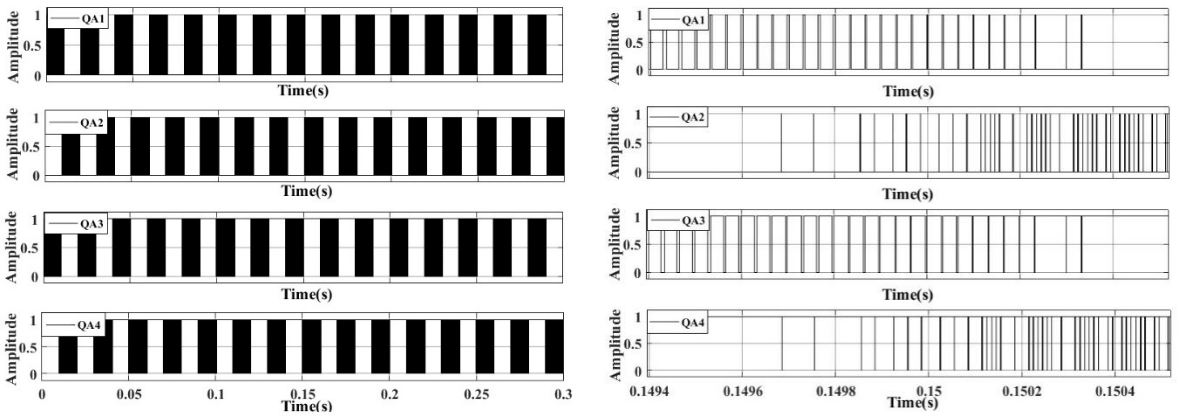
Table 1. Parameter setting of a simulation experiment

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|  | Circuit parameter type | Parameter value |
|  |  |  |
|  | AC input voltage (V) | 380 |
|  | DC output (V) | 800 |
|  | Rated power (KW) | 30, 000 |
|  | Switching frequency (kHz) | 100 |
|  | AC inductance (μH) | 720 |
|  | DC capacitance (μF) | 4, 000 |
|  | Load resistance (Ω) | 30 |
|  |  |  |

Based on the three operating modes of the T-type three-level converter analyzed in the previous section, to ensure that switching losses are reduced during the switching process of +0.5 Udc level, 0 level, and -0.5 Udc level, it is therefore ensured that only one switching tube is changed during each switching in the level switching process. The switching process continuously cycles between QA1QA4→QA3QA4→QA2QA3→QA3QA4.

Since the condition containing the closure of the Q A1 tube represents the +0.5 Udc level, the condition containing the closure of the QA2 tube represents the -0.5 Udc level and the condition with the simultaneous closure of QA3 and QA4 tubes represents the 0 level. Ideally, it is tried to ensure that the number of QA1 and QA2 tubes is equal, otherwise, the problem of unequal partial voltages of Capacitor 1 and Capacitor 2 on the bus side is caused.

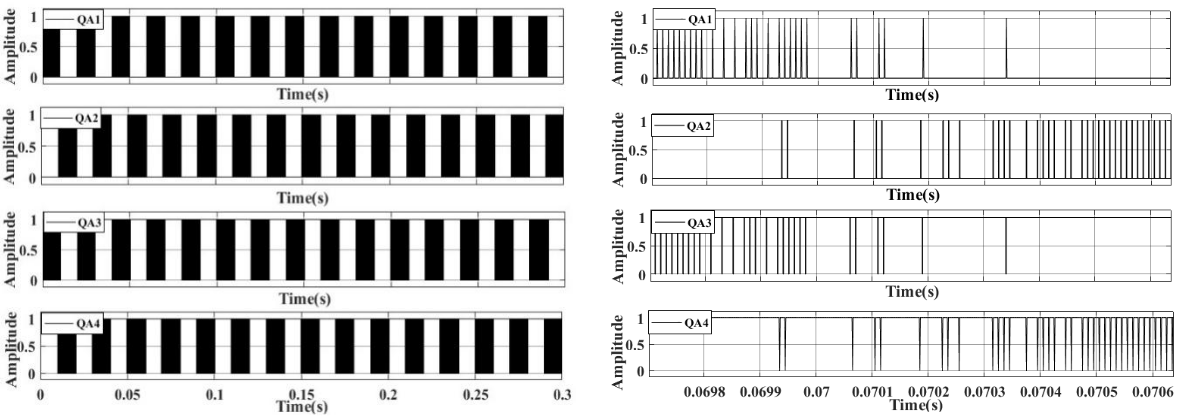
Therefore, the waveforms of the two modulation methods are intercepted and the local waveforms are extracted for comparison. Figure 8 shows the conventional three-level SPWM modulation waveform, Figure 9 shows the localized zoomed-in view of the conventional three -level SPWM modulation waveform, Figure 10 shows the simplified three-level SPWM modulation waveform, and Figure 11 shows the localized zoomed-in view of the simplified three-level SPWM modulation waveform.



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| Figure 8. Conventional three-level SPWM | Figure 9. Localized enlargement of conventional |
| modulation waveforms | three-level SPWM modulation waveforms |

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| Figure 10. Simplified three-level SPWM | Figure 11. Simplified three-level SPWM |
| modulation waveforms | modulation waveform with localized |
|  | enlargement |

By comparing the local magnification diagrams of different modulations, it can be seen that in the traditional three-level SPWM modulation, there is a large difference between the number of conditions containing QA1 tube closure and QA2 tube closure; on the contrary, the number of conditions containing QA1 tube closure and QA2 tube closure of the newly proposed simplified three-level SPWM modulation is approximately equal. Therefore, compared with the conventional three -level SPWM modulation, the simplified three -level SPWM modulation should be better optimized for the voltage dividing effect of Capacitor 1 and Capacitor 2 on the DC bus side.

To verify the accuracy of the above reasons, the voltage dividing waveforms of DC bus-side Capacitance 1 and Capacitance 2 corresponding to the two modulation methods were observed by using an oscilloscope, respectively. Figure 12 shows the waveforms of capacitance dividing corresponding to the conventional three- level SPWM modulation, and Figure 13 shows the waveforms of capacitance dividing corresponding to the simplified three-level SPWM modulation.

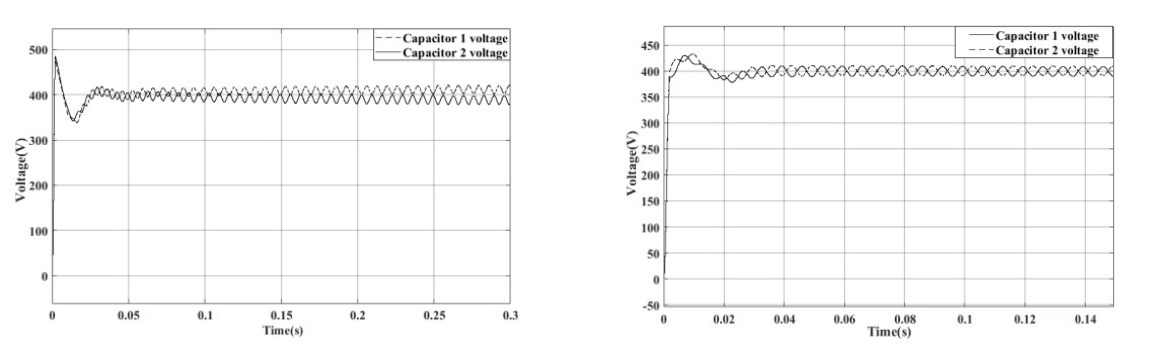


Figure 12. Conventional three- level SPWM modulation capacitor divider waveforms

Figure 13. Simplified three-level SPWM modulation capacitive divider waveforms

By comparison, it can be obtained that, based on the capacitance divider waveform obtained by the traditional three-level SPWM modulation, Capacitor 1 and Capacitor 2 voltages can be stabilized at

±410 V during the initial operation stage. With the prolongation of the working time, voltages of Capacitor 1 and Capacitor 2 begin to diverge gradually, and the voltage difference between Capacitor 1 and Capacitor 2 gradually increases with the prolongation of the working time; in contrast, based on the simplified three-level SPWM modulation based on the capacitor divider waveform obtained, voltages of Capacitor 1 and Capacitor 2 can be stabilized at ±410 V, and will not change with the change of time.

Therefore, by comparison, it can be concluded that: the traditional three -level SPWM modulation has a large difference between the number of working conditions containing QA1 tube closure and QA2

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tube closure, which results in a poorer optimization effect of voltage dividing between Capacitance 1 and Capacitance 2 on the DC bus side. The simplified three-level SPWM modulation has a similar number of working conditions containing QA1 tube closure and QA2 tube closure, which results in a lower optimization effect of voltage dividing between Capacitance 1 and Capacitance 2 on the DC bus side. The voltage division optimization effect is better for Capacitor 1 and Capacitor 2 on the DC bus side.

Compared with the conventional three-level SPWM modulation, the simplified three-level SPWM modulation corresponds to a neater and more standardized modulation waveform, fewer switching actions, and lower switching losses. Therefore the effect of bus voltage-current based on simplified three-level SPWM should be better than that of conventional three-level SPWM. To verify the accuracy of the above reasons, the DC bus voltage-current waveforms corresponding to different modulation methods and the waveforms corresponding to the conditions of sudden load change were observed by using an oscilloscope, respectively. Figure 14 is a voltage waveform based on a conventional three-level SPWM modulation method; Figure 15 is a current waveform based on a conventional three-level SPWM modulation method current waveform; Figure 16 is a voltage waveform based on a simplified three-level SPWM modulation method; Figure 17 is a current waveform based on a simplified three-level SPWM modulation method; Figure 18 is a voltage waveform based on a conventional three-level SPWM modulation load mutation voltage waveform; Figure 19 is a mutation voltage waveform based on a simplified three-level SPWM modulation load.

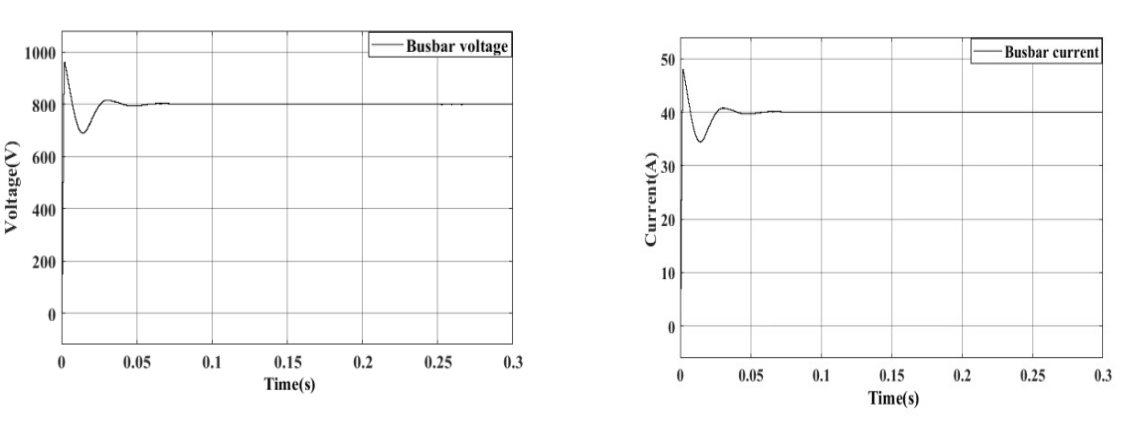


Figure 14. Conventional three-level SPWM

modulation voltage waveforms

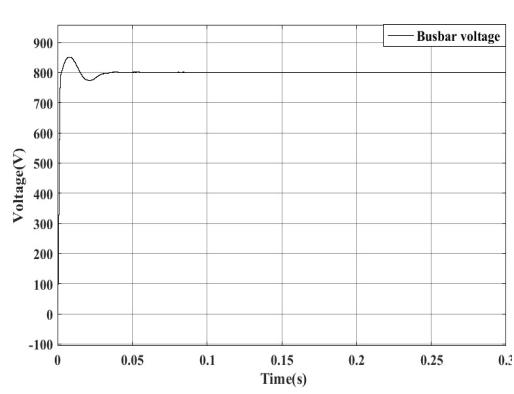
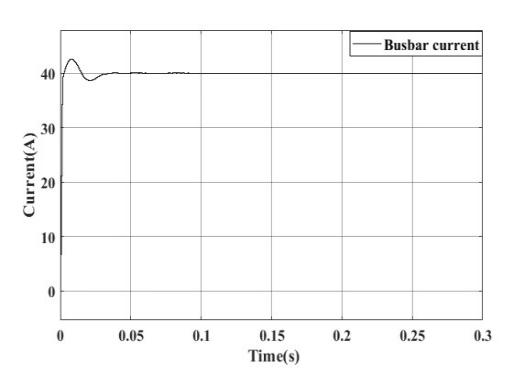


Figure 15. Conventional three-level SPWM

modulated current waveforms



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| Figure 16. Simplified three-level SPWM | Figure 17. Simplified three-level SPWM |
| modulation voltage waveforms | modulated current waveforms |

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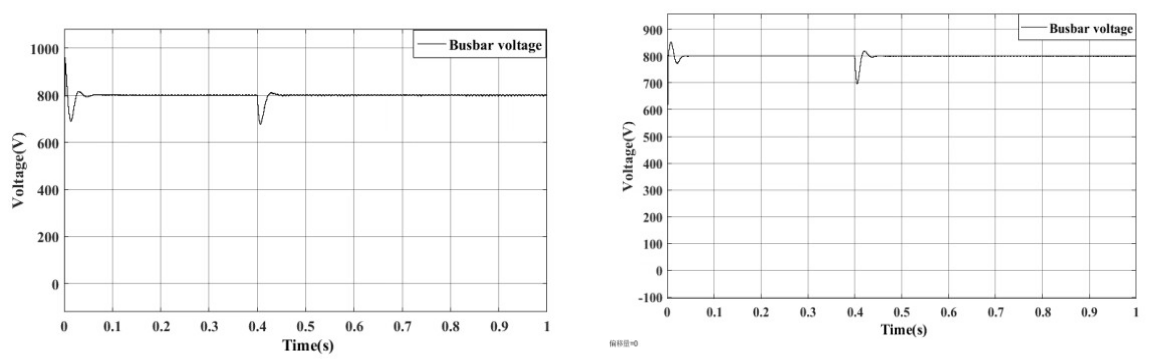


Figure 18. Conventional three-level SPWM

modulated load burst voltage waveforms

Figure 19. Simplified three-level SPWM modulated load burst voltage waveforms

Through the above comparison, due to the limitations of the traditional three -level SPWM modulation and the large difference in the number of modulating waveforms of different levels, the bus voltage and current have large overshoots and oscillations, and the bus voltage and current error are maintained at ±0.5, and it takes 0.1 second for the waveform to reach the steady state from the establishment; on the other hand, compared with the simplified three -level SPWM modulation, the simplified three-level SPWM modulation has the same modulating waveforms and standardized waveforms. On the contrary, for the simplified three -level SPWM modulation, due to the approximately equal number of modulated waveforms for different levels and the standardized modulation waveforms, the simplified three-level SPWM modulation is optimized for the overshooting of the DC bus voltage and current compared to the traditional three-level SPWM modulation, the bus voltage and current error is maintained at ±0.2, and it takes 0.05 seconds to run the waveforms from the establishment to the steady-state operation. Moreover, for the two different modulation modes, at the 0.001 level, it takes 0.1 seconds to run the waveforms from the establishment to the steady-state operation.

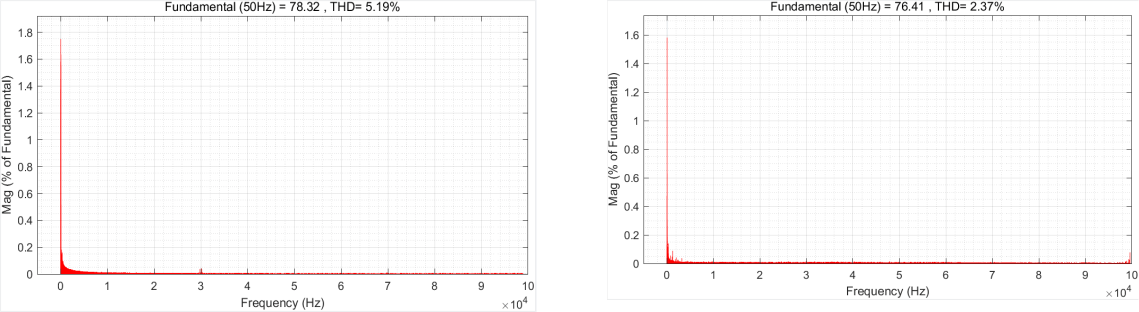
In addition, for the two different modulation modes, the load mutation is added at 0.4 seconds, and it is found that the voltage overshoot of the simplified three-level SPWM modulation is still lower than that of the traditional three- level SPWM modulation, and the recovery time after the load mutation is also shorter than that of the traditional three-level SPWM modulation by comparison. Thus, compared with the traditional three -level SPWM modulation, the simplified three-level SPWM modulation is better optimized based on the traditional three-level SPWM modulation.

Based on the comparison of the locally amplified waveforms of the two previous modulation methods, compared with the conventional three-level SPWM modulation, the switching action of the waveform of the simplified three-level SPWM modulation is less than that of the conventional three-level SPWM modulation, and thus the simplified three-level SPWM modulation method should reduce the switching loss and lower the THD value.

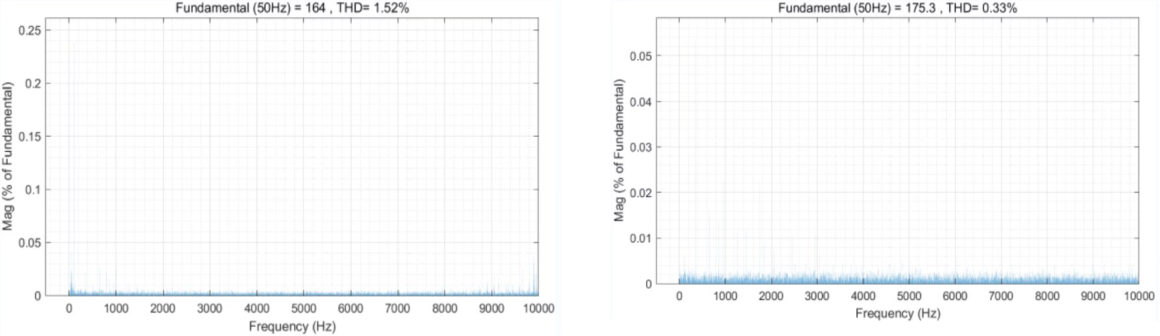
To verify the accuracy of the above analysis, the THD of the two modulation methods under different conditions were observed by using an oscilloscope respectively. Figure 20 is the THD waveform corresponding to the conventional three-level SPWM modulation based on the conventional three-level SPWM modulation; Figure 21 is the THD waveform corresponding to the simplified three-level SPWM modulation; Figure 22 is the THD waveform corresponding to the conventional three-level SPWM modulation based on the conventional three-level SPWM modulation after the addition of the load mutation; Figure 23 is the THD waveform corresponding to the simplified three-level SPWM modulation based on the load mutation after the addition of the load mutation.

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| Figure 20. Conventional three-level SPWM | Figure 21. Simplified three-level SPWM |  |
| modulation THD waveforms |  |
| modulation THD waveforms |  |
|  |  |



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| --- | --- | --- |
| Figure 22. Conventional three-level SPWM | Figure 23. Simplified three-level SPWM |  |
| modulation THD waveform (after load |  |
| modulation THD waveform (after load |  |
| mutation). |  |
| mutation) |  |
|  |  |

Combining the above comparisons and the analysis in the previous section, it can be seen that the simplified three-level SPWM modulation has fewer switching actions compared to the conventional three-level SPWM modulation, which reduces the switching loss to a certain extent and lowers the THD value.

**6. Conclusion**

In this paper, a simplified SPWM modulation algorithm for a T-type three-level converter is proposed, which is implemented on a single chip DSP28335. Currently, the method used to deal with three-level modulation is, on the one hand, the three-level SVPWM modulation technique, which has no requirement for the number of carriers, but the complexity of the three-level SVPWM modulation technique is much greater than that of the three-level SPWM modulation technique. With the increase of the number of levels, the difficulty of the algorithm increases exponentially, and the difference of the size vector synthesis method also causes the bias of the neutral point voltage of the dc-side capacitor, and the excessive bias will cause permanent damage to the dc-side components; on the other hand, it is to increase the cost of the hardware, and the use of multi-core chips aims to realize the three-level SPWM modulation. Therefore, a three- level simplified SPWM modulation is proposed in this paper, which realizes the three-level SPWM modulation without increasing the hardware cost and completes the optimization based on the traditional three-level modulation, optimizing the problem of uneven voltage division between the upper and lower capacitance of the bus side and reducing the switching loss and the overshooting of the bus voltage.

At present, the algorithm is only extended to three levels, and the extension to multi-level is an urgent problem to be solved and the direction of continuous efforts.

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