**DESIGN AND FPGA IMPLEMENTATION OF COMPENSATOR FOR SHARPENING CIC FILTER**

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**Abstract**. This paper presents a novel compensator design for sharpened CIC (cascade-integrator-comb) proposed in the literature. Sharpened CIC provides higher aliasing attenuation than the CIC filter. However, its passband droop is higher than the corresponding CIC filter and must be compensated. Our motivation was to design a decimator with better compensation than the one proposed in the literature. The proposed decimation filter has two coefficients and six adders. The coefficients are determined using particle swarm optimization (PSO) in MATLAB. Two designs are presented. The first one has two multipliers and six adders. The second is a multiplierless design obtained by presenting optimal coefficients in the signed power-of-two (SPT) form. The proposed design is compared with the design from the literature. The designed compensator is implemented in a field-programmable gate array (FPGA). Details of the implementation are described in the paper.

**1. Introduction**

Decreasing the sampling rate in the digital domain has many applications in communications, software-defined radio, and oversampled analog-digital converters, among others [1-4]. Decreasing the sampling rate introduces aliasing, which must be eliminated by the digital decimation or antialiasing filter [5]. The cascade-integrator-comb (CIC) filter is the simplest decimation multiplierless filter. The CIC filter must attenuate the aliasing in the bands around the filter’s zeros, called folding bands. As such, attenuation in the folding bands should be high. However, the attenuation provided by the CIC filter is insufficient, especially in the first folding band. Many authors proposed different methods to increase CIC aliasing rejection while trying to keep as much as possible its low complexity [6-11]. Additionally, since the CIC frequency characteristic in the passband of interest is not flat should be compensated by a filter called a compensator. The design of CIC compensators is presented, for example, in works [12-14]. The authors in [6] presented sharpening CIC filters to improve aliasing rejection and the compensators to decrease a high droop in the passband of interest. Different sharpened polynomials are considered, and the compensator designs for several passbands of interest. However, the compensators in [6] do not provide flexibility in design, and the compensator magnitude characteristic in dB is not zero for the zero frequency and should be normalized.

The work proposed here aims to improve the compensator design proposed in [6]. The first goal is to provide flexibility in the design by trading off the number of compensator adders and the compensation quality expressed in the absolute value of the maximum passband deviation in the passband of interest.

The next goal is to get a naturally normalized compensator characteristic. The rest of the paper is organized as described in the following. Section 2 briefly presents the minimax sharpened CIC filters and designed optimum coefficient compensators from [6]. Section 3 elaborates on the proposed compensator design and is illustrated with two examples. The comparison of the proposed design and the design from [6] is elaborated in Section 4. Section 5 presents the results of the FPGA design. Finally, the last section presents concluding remarks.

**2. Minimax sharpened CIC filters and optimum compensators**

This section briefly introduces the minimax sharpened CIC (SHCIC) filters and the designed corresponding optimum narrowband multiplierless compensators proposed in [6]. Four sharpening polynomials and the corresponding compensators for several passbands of interest are presented.

The coefficients of compensators are given in SPT (signed power-of-two forms). The number of adders varies from 4 to 8, and the corresponding values of the passband deviation vary from 0.03 dB to 0.24 dB, depending on the passband width of interest defined by the passband edge *ωp*. The method is illustrated in the following example.

**Example 1.** The sharpened polynomial *p*(*x*)=-2-6*x*2+*x*4, where *x* is the CIC filter. The passband of interest is defined by *ωp=π*/4*.* The compensator coefficients reported in [6] are given as, *g*=[-1-23, 2+26, -1-23]. Observe that the compensator coefficients should be normalized by the coefficient *K*= -1-23+2+26-1-23=-24+26.

The magnitude response of compensated SHCIC filter, denoted as | ( )|, is given as:

|  |  |  |
| --- | --- | --- |
| | | ( )| = | ( )| × | ( )|, | (1) |
|  |  |  |

where | ( )| and | ( )| are magnitude responses of the SHCIC filter and the compensator [6], respectively.

Figure 1 compares the magnitude responses of the no compensated and compensated SHCIC filters in the passband, taking the normalized compensator in [6].



**Figure 1.** Magnitude responses of no compensated and compensated SHCIC filters in [6].

2

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**3. Proposed compensator for minimax sharpened CIC**

The goal is to introduce a novel normalized compensator that exhibits a trade-off between the number of adders and the maximum absolute value of passband deviation *δ* in dB. We propose adapting the CIC compensator proposed in [14] to compensate for the SHCIC filter.

The magnitude characteristic of the compensator ( ) is in the sinusoidal form,

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | ( )| = 1 +4 | ( |  | ) + |  | 2 | ( |  | ), | (2) |  |
|  | 2 |  |  |
| 1 | 2 |  |  | 2 |  |  |  |
|  |  |  |  |  |  |  |

where *M* is the decimation factor, and *A*1 and *A*2 are the design parameters.

The system function of the compensator (2) has six adders and two coefficients, *C*0 and *C*1, [14]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  ( ) = (1 + −4 | − 2  | −2) + ( −1 | + −3 + 2 −2) + −2. | (3) |
| 0 |  | 1 |  |  |

The compensator coefficients *C*0 and *C*1 are obtained from the parameters *A*1 and *A*2 in (2) as [14]:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | = × 2−4. |  | = (  | + )×2−2. | (4) |
| 0 | 1 | 1 | 1 | 2 |  |

The number of compensator adders from (3) and (4) is

|  |  |
| --- | --- |
| *N*=6+*N*0+*N*1, | (5) |

where *N*0 and *N*1 are the numbers of adders in the compensator coefficients *C*0 and *C*1, respectively.

The magnitude response of compensated SHCIC filter, denoted as | ( )|, is given as:

|  |  |  |
| --- | --- | --- |
| | | ( )| = | ( )| × | ( )|, | (6) |
|  |  |  |

Using particle swarm optimization (PSO) in MATLAB [15] we get the optimum parameters *A*1*opt* and *A*2*opt* which give the optimum absolute deviation of (6) in the passband defined by the passband edge *ωp*.From (4) the optimum coefficients of the compensator are :

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | = | × 2−4. | = (  | + | 2  | )×2−2 . | (7) |  |
| 0  | 1  | 1  | 1  |  |  |  |  |

The compensator has six adders and two multipliers. To get a multiplierless design the optimum parameters 1  and 2  are presented in SPT (signed power-of-two) forms. The method is illustrated in the following example.

**Example 2.** We consider the same SHCIC as in Example 1. The optimal values of parameters are obtained as 1  = 0.5546, 2 =0.6674. The optimum value of the passband deviation is 0.0004 dB. Table 1 presents multiplierless design varying the number of adders from nine to eleven.

**Table 1**. SPT design parameters, compensator coefficients, number of adders *N*, and passband deviation

* in dB.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | SPT form of *A* | SPT form of *B* | *C*0 | *C*1 | N | *δ* in dB |
|  | 2-1+2-3-2-5 | 2-1+2-3+2-5 | 2-5+2-7-2-9 | 2-2+2-4 | 9 | 0.0067 |
|  | 2-1+2-3-2-5-2-7 | 2-1+2-3+2-5+2-7 | 2-5+2-7-2-9-2-11 | 2-2+2-4 | 10 | 0.0011 |
|  | 2-1+2-4-2-6+2-8 | 20-2-2-2-4-2-6-2-8 | 2-3+2-6-2-8+2-10 | 2-3+22+24 | 11 | 0.00056071 |

Magnitude responses of the compensated SHCIC filter with the optimum compensator and compensators from Table 1 are contrasted in Figure. 2.

3

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**Figure 2.** Magnitude responses in the passband of the compensated SHCIC using the designs from Table 1.

**Example 3**. We design the compensator for the sharpening polynomial *p*(*x*)=2-10*x*2-2-4*x*4+*x*6, for *ωp*=*π*/3.

The optimum values of the parameters of design are 1  = 1.2459, 2 =0.9919, while *δ*opt=0.0055 dB. Table 2 presents the results of the multiplierless design, varying the number of adders from eight to ten. We can observe that the choice of *N*=10 equals practically to the optimum design.

**Table 2**. SPT design parameters, compensator coefficients, number of adders *N*, and passband deviation in dB.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | SPT form of *A* | SPT form of *B* | *C*0 | *C*1 | N | *δ* in dB |
|  | 20+2-2 | 20 | 2-4+2-6 | 2-1+2-4 | 8 | 0.0166 |
|  | 20+2-2 | 20-2-7 | 2-4+2-6 | 2-1+2-4-2-9 | 9 | 0.0062 |
|  | 20+2-2 | 20-2-7-2-11 | 2-4+2-6 | 2-1+2-4-2-9-2-13 | 10 | 0.0056 |

Figure 3 contrasts the magnitude responses of the compensated SHCIC filters in the passband.

**4. Comparisons with method in [6]**

In this section we compare the proposed design with the method in [6] in the following examples.

**Example 4.** We compare the proposed design with the design in [6] given in Example 1. We take the design parameters from the first row of the Table 1. The values of the maximum passband deviations in

1. and the proposed design are 0.03 dB and 0.0067 dB, respectively, while the required numbers of adders are four, and nine, respectively.

The corresponding magnitude responses in the passband are contrasted in Figure 4. It can be observed that the proposed design achieves much better characteristic in the passband at an expense of the increased number of adders.

4

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**Figure 3**. Magnitude responses in the passband of the compensated SHCIC using the designs from Table 2.



**Figure 4**. Comparison with the compensated SHCIC [6] and the proposed compensated SHCIC from Table 2.

**Example 5.** We compare the proposed design from the first row in Table 2 with the second design in

1. The values of the maximum absolute values of the passband deviations, in [6] and the proposed design, are 0.0285 dB and 0.0166 dB, while the corresponding numbers of adders are five and eight. The magnitude responses in passbands are contrasted in Figure 5.

5

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**Figure 5.** Comparison with the compensated SHCIC [6] and the proposed compensated SHCIC from Table 2.

**5. FPGA implementation**

The compensator was implemented in FPGA on an EP235F672 card using Quartus II software, designed to observe the impulse response, which impulse response has been generated from the FPGA itself.

Figure 6a shows the block diagram that was proposed to carry out the multiplication with *C*o in equation (3), denoted as *M*0, while Figure 6b shows the diagram provided by the Quartus II software. In a very similar way, block diagrams of multiplication with *C*1, denoted *M*1, in equation (3) are presented in Figure 6c. Similarly, Figure 6d shows the diagram provided by the Quartus II software.



(a)



(b)

6

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(c)



(d)

**Figure. 6.** Implementation of system function given in equation (3).

Figure 7 shows the highest hierarchy RTL diagram of the compensator implemented in the FPGA. The circuit is made up of 6 blocks. The first block "filter pulse:V4" generates a unit pulse as input to the system. The "filter\_regs:V1" block are the shift registers, to delay the signal; at the output we have the four delayed signals, from one to four samples to use them as inputs to the operator blocks, "filter\_c0:V2" and "filter\_c1: V3” that represent the implementation of *M*0 and *M*1 respectively. The subtraction is made in the "filter\_sub:V5" block, and finally the result is added with the signal *Z*2 to obtain the output of the compensator.



**Figure 7**. RTL diagram of the implemented compensator.

Summary of power and resource consumption is given in Figure 8.



(a) Power consumption.

7

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* 1. Resource consumption. **Figure 8**. Summary of power and resource consumption.
1. **Conclusion**

We present the design and FPGA implementation of the narrowband compensator for SHCIC filter proposed in the literature. The proposed compensator presents better passband compensation and is naturally normalized in the comparison with the designs given in [6].

The proposed design generally requires higher number of adders. However, since the compensator works at low rate, the complexity of the compensator is unsignificantly increased.

Additionally, the proposed design exhibits the flexibility expressed in the trade-off between the number of adders and maximum value of the deviation in the passband.

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8

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9